REMARKS

With respect to the Office Action at page 5, Applicant notes that dependent claims 2, 3, 7-12, 14 and 17-20 would be **allowable** if rewritten to overcome the rejection under 35 U.S.C. §112, second paragraph, and to include all of the limitations of a base claim and any intervening claims. Applicant has amended these claims to overcome the rejection under 35 U.S.C. §112, second paragraph, and respectfully requests the Examiner to hold in **abeyance** the rewriting of these claims in independent form until the Examiner has had an opportunity to reconsider (and withdraw) the prior art rejections of independent claim 1 and dependent claims 4-6 and 13.

Claim 15 (15/1) is not rejected on prior art, but the Examiner did not explicitly list the claim as one which would be allowable if rewritten in independent form. Thus, Applicant requests the Examiner to hold in abeyance the rewriting of claim 15 (15/1).

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Woolaway '511. Such a rejection requires that Woolaway disclose, either expressly or inherently, each limitation of claim 1, or in other words, that claim 1 be readable on Woolaway's disclosure. Applicant respectfully submits that clearly such is **not** the case here with respect to amended claim 1.

More specifically, claim 1 has been amended to include those limitations of claim 2 which form the basis for the Examiner's reasons for allowance of claim 2: "an output stage comprising a gate terminal connected to the operational amplifier output and an output terminal connected to said first terminal of the integrating voltage storage device" (paragraph bridging pages 5 and 6 of the Office Action).

Thus, this statutory rejection of claim 1 has been rendered moot by the above amendments which insert in claim 1 the salient limitations of claim 2.

Since the **amended claim 1 is allowable** over the prior art, then all of its dependent claims 2-15 also should, by definition, be allowable over the prior art.

In this regard, claim 2 has been amended to delete therefrom the salient features which were added to parent claim 1.

Since parent claim 1 now contains novel and unobvious limitations from original claim 2, the rejections of dependent claims 4-6 and 13 under 35 U.S.C. § 103(a), based on unpatentability (obviousness) over Woolaway '511 alone, or in combination with the secondary references Marion '248, Pain '413 and Chen '039, have been **overcome** because this prior art does not make the subject matter of each of these claims *prima facie* obvious under 35 U.S.C. § 103(a).

Turning now to the questions raised by the Examiner under the heading Claim Rejections - 35 U.S.C. § 112, Applicant respectfully traverses the Examiner's belief concerning the term "balancing". In fact, the term "balancing" or the corresponding verb form, "to balance", is well-known to those skilled in the art and can be found in any electronic dictionary with more or less the same following definition: equalizing two loads, voltages or signals between two circuits, components or terminals.

Furthermore, it seems that the Examiner has no difficulty in understanding this term, since the Examiner finds said balancing means in Woolaway (col.3 lines 44-45) which effectively discloses "means for balancing" in accordance with the aforementioned well-known definition.

In the present application, this "balancing" effect is obtained with the first switching device 51 that connects the operational amplifier output to the operational amplifier inverting input during the reset phase.

Therefore, for the sake of clarity **in claims 1 and 16,** Applicant replaces:

"means for balancing said operational amplifier" with

"a first switching device for connecting said operational amplifier output to said operational amplifier inverting input during said reset phase".

Concerning the other ground of rejection under 35 USC § 112, it is clear from Applicant's specification (see, in particular, the paragraph bridging pages 7 and 8) that on the one hand, "a voltage substantially equal to bias voltage **$V_{PD\text{-}BIAS}$ is applied across device 25**", which means that the potential difference between both terminals of the integrating voltage storage device is substantially equal to bias voltage $V_{PD\text{-}BIAS}$. And on the other hand, "At the same time [i.e., also during the reset phase], the integrating circuit output OUT is pulled to a reference potential". Since the integrating circuit output is connected to the first terminal of the integrating voltage storage device, this latter also is pulled to the reference potential during the reset phase.

Therefore, there is no contradiction in the facts that the voltage, applied across said integrating voltage storage device, is $V_{PD\text{-}BIAS}$, and that the first terminal of said integrating voltage storage device is pulled to a potential reference in the meantime, i.e., during the reset phase.

However, again for the sake of clarity **in claims 1 and 16**, Applicant replaces:

"means for (...) developing a voltage across said integrating voltage storage device during said reset phase, which voltage is substantially equal to said bias voltage, said first terminal of the integrating voltage storage device being pulled to a reference potential during said reset phase" with:

"means for resetting said integrating voltage storage device during said reset phase, a voltage equal to said bias voltage being applied across said integrating voltage storage device and said first terminal of said integrating voltage storage device being pulled to a reference potential".

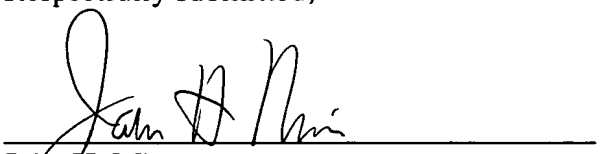
Finally, in order to clarify the syntax of **claim 13**, the first and second "source-follower output stages" now are separately recited: A first source-follower output stage provides minimum electrical output signal allowing determination of the optical sensor within the array with the least intensity, and a second source-follower output stage provides a maximum electrical output signal allowing determination of the optical sensor within with the greatest intensity.

In summary, then, Applicant respectfully requests the Examiner to reconsider and withdraw the rejections under 35 U.S.C. §§ 112, 102 and 103(a), and to find the application to be in condition for allowance with all of claims 1-20; however, if for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to **call the undersigned attorney** to discuss any unresolved issues and to expedite the disposition of the application.

Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this application, and any required fee for such extension is to be charged to

Deposit Account No. 19-4880. The Commissioner is also authorized to charge any additional fees under 37 C.F.R. § 1.16 and/or § 1.17 necessary to keep this application pending in the Patent and Trademark Office or credit any overpayment to said Deposit Account No. 19-4880.

Respectfully submitted,



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